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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,147	11/25/2003	Michael A. Walker	11675.102.2	6315

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/721,147	WALKER ET AL.
	Examiner	Art Unit
	Michael Trinh	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 November 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7-19-2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on November 25, 2003. Claims 1-7 are pending.

Specification

1. Specification page 1, paragraph [001], updating status information of parent application Serial No. 09/012,388 as " now abandoned" is respectfully requested.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1,2,4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Morie et al (4,786,954).

Re claim 1, Morie teaches a method for an interconnect in an oxide isolation region immediately adjacent to an active area of an integrated circuit, comprising: masking the active area with the nitride layer 16, wherein an edge of the nitride layer 16, as shown in Figure 6D-6C, is aligned with a lateral edge of the active area 1 of P-type conductivity that abuts the oxide isolation region 40 (Figs 6D-6C; col 5, line 50 through col 6, line 15); exposing the oxide isolation region 40 and a portion of the nitride layer 16 to an etch process that etches the oxide isolation region 40 faster than the nitride layer 16 such that a portion of the oxide isolation region 40 is removed to form a downwardly extending opening in the oxide isolation region 40 that exposes a portion of the lateral edge of the active area 1 (Fig 6F-6G; col 6, line 16-52); and at least partially filling the opening with a polysilicon material 13 such that the polysilicon material contacts the active area 14,62 (Figs 6H-6I; col 6, lines 53-66). Re further claim 2,

wherein the oxide dielectric isolation region 40 and the active silicon area 1 of the integrated circuit share a common vertical interface, wherein lateral edge of the nitride layer 16 is aligned with a lateral edge of the active silicon area 1 along the common vertical interface. Re further claim 4, wherein the nitride layer 16 is vertically separated from the active area 1 by a layer 15 of oxide (col 5, lines 55-62; Figs 6D-6C). Re further claim 3, wherein the method of Morie comprises providing a vertical edge of an active area 1 with an integrated circuit substrate assembly; forming a region of dielectric material 40 immediately adjacent to and in contact with the vertical edge of the active area 1 of P-type conductivity; forming a nitride layer 16 above the active area 1 and in alignment with the vertical edge (as shown in Figs 6D-6C, col 5, line 50 through col 6, line 15); etching a hole into the region of the dielectric material 40 at the vertical edge, wherein the hole is etched with an etching process that selectively etches the region of the dielectric material 40 at a faster rate than the etching process etches the nitride layer such that the active area 1 is not etched (Fig 6F-6G; col 6, line 16-52); and filling at least a portion of the hole with a volume of electrically conductive material 13 with the region of the dielectric material, the volume of electrically conductive material being situated in contact with the vertical edge 14,62, the region of the dielectric material making planar interface in contact with the vertical edge (Figs 6G-6I; col 6, lines 53-66; col 7). Re claim 6, wherein etching a trench through a sacrificial covering layer 15,16, and filling the trench with a dielectric material 40 (Figs 6B-6E; col 5, line 52 through col 6). Re further claim 7, wherein the method of Morie comprises forming a silicon nitride layer 16 above a silicon substrate 1 of the integrated circuit; etching a trench through the silicon nitride layer 16 and into the silicon substrate 1 to expose a vertical edge within the silicon substrate that is orthogonal to a top plane of the substrate (as shown in Figs 6B-6D, col 5, line 50 through col 6, line 23); filling the trench with a dielectric material 40/18 to form an isolation region; etching a hole into the isolation region at the vertical edge with an anisotropic RIE etch to selectively etch the dielectric material at a faster rate than the etching process etches the nitride layer (Fig 6E-6G; col 6, lines 33-52); forming a polysilicon plug 13 within at least a portion of the hole such that the polysilicon plug is situated to the side of, in contact with, and immediately adjacent to the vertical edge and such that the polysilicon plug forms a planar and vertical interface 14 with the silicon substrate 1 (Figs 6G-

6I; col 6, lines 53-66; col 7); and implanting dopants into the silicon substrate to form an active region 61 adjacent the vertical interface (Fig 6N; col 8, lines 13-17).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morie et al (4,786,954) taken with Pfiester (5,166,084).

Morie teaches a method for an interconnect as applied to claims 1,2,4-7 above.

Morie teaches forming the dielectric isolation region comprising thermal oxide while, as recited in claim 3, the dielectric isolation region comprises borophosphosilicate glass.

However, Pfiester teaches (at col 6, lines 33-38) forming a dielectric layer by alternatively using thermal oxide growth of silicon dioxide or a borophosphate-silicate glass.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric region of Morie by using either the thermal oxide growth of silicon dioxide or the borophosphate-silicate glass, as taught by Pfiester. This is because these high quality dielectric material are alternative and art recognized equivalent materials for substitution in forming dielectric regions used for electrically isolating active regions from being unwanted connection.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

7. Claims 1-7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-52 of U.S. Patent No. 6,168,986. Although the conflicting claims are not identical, they are not patentably distinct from each other because this present application and the Patent are drawn to the same invention, in which scope of claims 1-7 of this present application are anticipated and broad enough to encompass the scope of claims 1-52 of the Patent No. 6,168,986 (at col 12, line 58 through col 16; present claim 7 is respectively anticipated by claim 30 of the Patent; at column 15, lines 18-55), and in which active region (col 14, lines 1-2) is masked by a silicon nitride layer (col 15, lines 20-21; col 14, lines 63-65; col 13, lines 40-44); wherein etching and filling the trench with a dielectric film are mentioned at col 15, lines 21-34); wherein etching a hole in isolation regions at a faster rate than the nitride layer (col 14,lines 39-45; col 13, lines 12-17; col 15, lines 28-34); wherein forming polysilicon plug is filling the hole (col 15, lines 35-40); wherein implanting dopants is mentioned at col 15, lines 44-47.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-102

Michael Trinh
Primary Examiner